Claim Amendments

1. (currently amended) A printed circuit board (PCB) comprising:

a first layer of electrically non-conductive material; and

~~a bond pad comprising~~ a patterned electrically conductive second material disposed in contact with ~~upon~~ said first layer, said electrically conductive second material forming a patterned bond pad defining a channel therein facilitating outgassing of bubbles via the channel, said first layer of electrically non-conductive material exposed in said channel through said patterned electrically conductive second material.

2. (original) The PCB as specified in Claim 1 wherein said bond pad is dimensioned to render said pad non-planar.

3. (original) The PCB as specified in Claim 1 wherein said bond pad is dimensioned to define a plurality of said channels extending laterally through said bond pad.

4. (original) The PCB as specified in Claim 1 further comprising a plurality of pads disposed about said bond pad and being adapted to receive a multi-pin integrated circuit being centered over the bond pad.

5. (original) The PCB as specified in Claim 3 wherein said channels are defined in a radial pattern.

6. (original) The PCB as specified in Claim 5 wherein said radial lines terminate at a point distant from a focal point.

7. (original) The PCB as specified in Claim 6 wherein said radial lines have different lengths.

8. (withdrawn) The PCB as specified in Claim 6 wherein some of the radial lines terminate different distances from the focal point.

9. (original) The PCB as specified in Claim 4 wherein said channels are defined as multiple lines.

10. (withdrawn) The PCB as specified in Claim 9 wherein said channels are defined as parallel said lines.

11. (withdrawn) The PCB as specified in Claim 9 wherein said multiple lines intersect.

12. (currently amended) In combination;

an integrated circuit having a lower surface including an exposed solder pad;

a first layer of electrically non-conductive material; and

~~a bond pad opposed said contact pad and comprising~~ a patterned electrically conductive second material disposed in contact with ~~upon~~ said first layer and opposed to said solder pad, said patterned electrically conductive second material forming a bond pad defining a channel therein facilitating outgassing of bubbles via the channel, said first layer of electrically non-conductive material exposed in said channel through said patterned electrically conductive second material.

13. (original) The PCB as specified in Claim 12 wherein said bond pad is dimensioned to render said pad non-planar.

14. (original) The PCB as specified in Claim 12 wherein said bond pad is dimensioned to define a plurality of said channels extending laterally through said bond pad.

15. (original) The PCB as specified in Claim 12 wherein said channels are defined in a radial pattern.

16. (original) The PCB as specified in Claim 12 wherein said channels are defined as multiple lines.

17. (withdrawn) A method of fabricating a printed circuit board (PCB) having electrically conductive signal traces thereon, comprising the steps of:

defining and patterning a bond pad to define a channel laterally through the bond pad adapted to facilitate outgassing of bubbles generated in solder during re-flow of solder upon the bond pad.

18. (withdrawn) The method of fabricating as specified in Claim 17 wherein the bond pad is dimensioned to render the bond pad non-planar.

REMARKS

Reconsideration of the above-referenced application in view of the following remarks is respectfully requested.

Claims 1-18 are pending in this application. Claims 8, 10, 11, 17, and 18 have been withdrawn from consideration.

Claims 1 and 12 stand rejected under 35 U.S.C. 112, second paragraph. Claims 1 and 12 have been amended to better define the scope of the claimed invention.

Claims 1-4, 9, 12-14, and 16 stand rejected under 35 U.S.C. 102(e) as being anticipated by Downey, et al. (U.S. Patent No. 6,362,435). Claim 1 as amended includes the feature of "a patterned electrically conductive second material disposed in contact with said first layer, said electrically conductive second material forming a patterned bond pad defining a channel therein facilitating outgassing of bubbles via the channel, said first layer of electrically non-conductive material exposed in said channel through said patterned electrically conductive second material." Downey does not disclose such a feature. In contrast to the claimed invention, Downey discloses a multi-layer conductor pad formed on a substrate. It is Downey's base layer (e.g. layer 12) that is in contact with substrate 11, not the patterned layer 16. Claim 12 includes a similar feature. Therefore, Applicant respectfully submits that Claims 1 and 12 are patentable over Downey. Claims 2-4, 9, 13, 14, and 16 depend from Claims 1 and 12 and are therefore patentable over Downey at least by virtue of their dependence from patentable base claims.

Claims 5-7, 15, and 16 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Downey and further in view of Ziemkowski, (U.S. Patent No.

6,294,742) and Chen (U.S. Patent No. 6,246,587). Claims 5-7, 15, and 16 depend from Claims 1 and 12. Claims 1 and 12 are distinguished from Downey above. Ziemkowski is cited for its teaching of a solder pad with a radial pattern. However, note that in Ziemkowski's Figure 1A, the power MOSFET device is mounted on a portion of the pad that lacks the radial trenches. The trenches therefore could play no role in providing a means for outgassing of bubbles, and the skilled artisan would lack any motivation to combine the teachings of Ziemkowski and Downey to arrive at the claimed inventions. Chen similarly fails to cure the deficiencies of Downey and Ziemkowski. Note that Chen's grooves 217 are cut only partially into pads 204 and 206 and thus a first layer of electrically non-conductive material is not exposed through channels in a second layer of electrically conductive material. Therefore, Applicant respectfully submits that Claims 5-7, 15, and 16 are patentable over the cited combination of references.

Claims 1-4, 9, 12-14, and 16 stand rejected under 35 U.S.C. 102(b) as being anticipated by Shigehiro Yamada (Japanese Patent No. JP02000260788A). Claim 1 as amended includes the feature of "a patterned electrically conductive second material disposed in contact with said first layer, said electrically conductive second material forming a patterned bond pad defining a channel therein facilitating outgassing of bubbles via the channel, said first layer of electrically non-conductive material exposed in said channel through said patterned electrically conductive second material." Yamada does not disclose such a feature. Yamada's grooves 13 are cut only partially into "die-bonding part" 12. Therefore a first layer of electrically non-conductive material is not exposed through channels in a second layer of electrically conductive material. Claim 12 includes a feature similar to that cited above from Claim 1. Therefore, Applicant respectfully submits that Claims 1 and 12 are patentable over Yamada. Claims 2-4, 9, 13, 14, and 16 are patentable over Yamada at least by virtue of their dependence from a patentable base claim.

Claims 5-7 and 15 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Yamada, and further in view of Ziemkowski and Chen. Claims 5-7, and 15 depend from Claims 1 and 12. Claims 1 and 12 are distinguished from Yamada above. Ziemkowski is cited for its teaching of a solder pad with a radial pattern. However, note that in Ziemkowski's Figure 1A, the power MOSFET device is mounted on a portion of the pad that lacks the radial trenches. The trenches therefore could play no role in providing a means for outgassing of bubbles, and the skilled artisan would lack any motivation to combine the teachings of Ziemkowski and Yamada to arrive at the claimed inventions. Chen similarly fails to cure the deficiencies of Yamada and Ziemkowski. Note that Chen's grooves 217 are cut only partially into pads 204 and 206, as in Yamada, and thus a first layer of electrically non-conductive material is not exposed through channels in a second layer of electrically conductive material. Therefore, Applicant respectfully submits that Claims 5-7, 15, and 16 are patentable over the cited combination of references.

Applicant respectfully requests reconsideration and withdrawal of the rejections and allowance of Claims 1-7, 9, and 12-16. If the Examiner has any questions or other correspondence regarding this application, Applicant requests that the Examiner contact Applicant's attorney at the below listed telephone number and address.

Respectfully submitted,

Texas Instruments Incorporated
P.O. Box 655474, M/S 3999
Dallas, TX 75265
Phone: 972 917-5653
Fax: 972 917-4418

Michael K. Skrehot
Reg. No. 36,682